

512MB 184Pin Unbuffered Dual Inline SDRAM Module (DIMM) DDR PC1600 / PC2100 / PC2700

Features

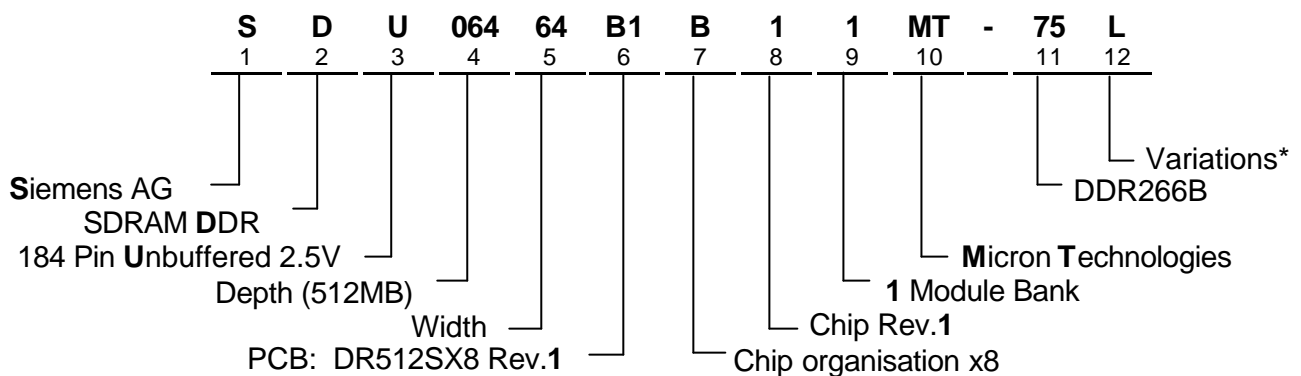
- 184 Pin Dual-In-Line Double Data Rate Synchronous DRAM Module
- 64Mx64 or 64x72 (ECC) organization
 - two bank module utilizing 32Mx8 DDR SDRAM components
- Intended for 100MHz (DDR200), 133MHz (DDR266) and 166MHz (DDR333) applications
- $V_{DD} = 2.5V \pm 0.2V$, $V_{DDQ} = 2.5V \pm 0.2V$
- SDRAM has 4 internal banks for concurrent operation
- All Inputs, Outputs are SSTL_2 compatible
- Internal double data rate architecture → data access on both clock edges
- Differential Clock Inputs
- Commands are synchronous to positive clock edge
- Programmable Operations:
 - CAS Latency: 2.0 or 2.5
 - Burst Type: Sequential or Interleave
 - Burst Length: 2, 4 or 8
 - Burst Read and Write
- Auto Precharge Option
- Auto Refresh (CBR) and Self Refresh Modes
- 7.8µs max. average periodic refresh interval
- Serial Present Detect (SPD)
- SDRAM packaged in 66-Pin TSOP Type II
- Gold contact pad
- Operating Temperature: 0°C to 70°C

Performance

Part No. – Speed Grade	Clock Frequency		DQ Burst Frequency		Clock cycle	
	CL = 2	CL = 2.5	CL = 2	CL = 2.5	CL = 2	CL = 2.5
SDU06464B1B.. – 80 PC1600	100 MHz	100 MHz	200 MHz	200 MHz	10.0 ns	10.0 ns
SDU06464B1B.. – 75 * PC2100	100 MHz	133 MHz	200 MHz	266 MHz	10.0 ns	7.5 ns
SDU06464B1B.. – 70 PC2100	133 MHz	143 MHz	266 MHz	300 MHz	7.5 ns	7.0 ns
SDU06464B1B.. – 60 PC2700	133 MHz	166 MHz	266 MHz	333 MHz	7.5 ns	6.0 ns

*Standard Module programmed PC2100-CL2.5 and PC1600-CL2

Part Number



* optional / additional information

Note:

Because SDRAM components from several suppliers are used, there exist also different Part Numbers for a Module of the same capacity and speed performance. Main DDR suppliers of Siemens Switzerland Ltd. are Micron Technologies (MT). Other suppliers, like Infineon(IN), Samsung(SA) or Nanya(NA), are available on request as well.

PCB details

Part No.	Organisation	Chip organisation	Number of chips	Banks	Board Size
DR1GBDX8	32x64 / 72 (ECC)	X8	8 or 9 (ECC)	2	1.25" x 5.25"

Pin Configuration

Frontside	
PIN#	Symbol
1	VREF
2	DQ0
3	VSS
4	DQ1
5	DQS0
6	DQ2
7	VDD
8	DQ3
9	NC
10	NC
11	VSS
12	DQ8
13	DQ9
14	DQS1
15	VDDQ
16	CLK1
17	CLK1
18	VSS
19	DQ10
20	DQ11
21	CKE0
22	VDDQ
23	DQ16
24	DQ17
25	DQS2
26	VSS
27	A9
28	DQ18
29	A7
30	VDDQ
31	DQ19
32	A5
33	DQ24
34	VSS
35	DQ25
36	DQS3
37	A4
38	VDD
39	DQ26
40	DQ27
41	A2
42	VSS
43	A1
44	NC / CB0
45	NC / CB1
46	VDD
47	NC / DQS8

Frontside	
PIN#	Symbol
48	A0
49	NC / CB2
50	VSS
51	NC / CB3
52	BA1
KEY	
53	DQ32
54	VDDQ
55	DQ33
56	DQS4
57	DQ34
58	VSS
59	BA0
60	DQ35
61	DQ40
62	VDDQ
63	WE
64	DQ41
65	CAS
66	VSS
67	DQS5
68	DQ42
69	DQ43
70	VDD
70	NC
72	DQ48
73	DQ49
74	VSS
75	CLK2
76	CLK2
77	VDDQ
78	DQS6
79	DQ50
80	DQ51
81	VSS
82	VDDID
83	DQ56
84	DQ57
85	VDD
86	DQS7
87	DQ58
88	DQ59
89	VSS
90	NC
91	SDA
92	SCL

Backside	
PIN#	Symbol
93	VSS
94	DQ4
95	DQ5
96	VDDQ
97	DM0 / DQS9
98	DQ6
99	DQ7
100	VSS
101	NC
102	NC
103	NC
104	VDDQ
105	DQ12
106	DQ13
107	DM1 / DQS10
108	VDD
109	DQ14
110	DQ15
111	CKE1
112	VDDQ
113	NC (BA2)
114	DQ20
115	NC / A12
116	VSS
117	DQ21
118	A11
119	DM2 / DQS11
120	VDD
121	DQ22
122	A8
123	DQ23
124	VSS
125	A8
126	DQ28
127	DQ29
128	VDDQ
129	DM3 / DQS12
130	A3
131	DQ30
132	VSS
133	DQ31
134	NC / CB4
135	NC / CB5
136	VDDQ
137	CK0
138	CK0
139	VSS

Backside	
PIN#	Symbol
140	NC / DM8 / DQS17
141	A10
142	NC / CB6
143	VDDQ
144	NC / CB7
KEY	
145	VSS
146	DQ36
147	DQ37
148	VDD
149	DM4 / DQS13
150	DQ38
151	DQ39
152	VSS
153	DQ44
154	RAS
155	DQ45
156	VDDQ
157	S0
158	S1
159	DM5 / DQS14
160	VSS
161	DQ46
162	DQ47
163	NC
164	VDDQ
165	DQ52
166	DQ53
167	NC (A13)
168	VDD
169	DM6 / DQS16
170	DQ54
171	DQ55
172	VDDQ
173	NC
174	DQ60
175	DQ61
176	VSS
177	DM7 / DQS16
178	DQ62
179	DQ63
180	VDDQ
181	SA0
182	SA1
183	SA2
184	VDDSPD

PIN Description

CK0-CK2	Differential Clock Inputs	DQ0 – DQ63	Data input / output
CKE0	Clock Enable	DQS0 – DQS7, DQS9 – DQS16	Bidirectional data strobe
RAS	Row Address Strobe		
CAS	Column Address Strobe	VDD	Power (2.5V)
WE	Write Enable	VDDQ	Supply voltage for DQ's (2.5V)
S0	Chip Selects	VSS	Ground
A0 – A11, A13	Address Inputs	NC	No Connect
A10 / AP	Address Input / Autoprecharge	SCL	Serial Presence Detect Clock Input
BA0, BA1	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input / output
VREF	Ref.Voltage for SSTL_2 inputs	SA0 - 2	Serial Presence Detect Address Inputs
VDDID	VDD Identification flag. (Not used when VDD = VDDQ	VDDSPD	Serial EEPROM positive power supply (2.5V)

SPD Table / AC Characteristics

SERIAL PRESENCE-DETECT MATRIX

Byte	DESCRIPTION	ENTRY			HEX Code		
		-60	-75 -70	-80	-60	-75 -70	-80
0	NUMBER OF BYTES USED	128			80		
1	TOTAL NUMBER OF SPD MEMORY BYTES	256			08		
2	MEMORY TYPE	SDRAM DDR			07		
3	NUMBER OF ROW ADDRESSES	13			0D		
4	NUMBER OF COLUMN ADDRESSES	10			0A		
5	NUMBER OF BANKS	2			02		
6	MODULE DATA WIDTH	64 or 72			40 or 48		
7	MODULE DATA WIDTH (continued)	0			00		
8	MODULE VOLTAGE INTERFACE LEVELS	SSTL_2 2.5V			04		
9	SDRAM CYCLE TIME ^t CK	6.0ns	7.5ns 7.0ns	8.0ns	60	75 70	80
10	SDRAM ACCESS TIME FROM CLOCK (CL=2.5)	0.70ns	0.75ns	0.8ns	70	75	80
11	MODULE CONFIGURATION TYPE	NONE or ECC			00 or 02		
12	REFRESH RATE / TYPE	7.8ms			82		
13	SDRAM WIDTH (PRIMARY SDRAM)	x8			08		
14	ERROR-CHECKING SDRAM DATA WIDTH	NONE or x8			00 or 0F		
15	MINIMUM CLOCK DELAY, ^t CCD	<i>t_{ccd} = CKL 1</i>			01		
16	BURST LENGTH SUPPORTED	2,4,8			0E		
17	NUMBER OF BANKS ON SDDRAM DEVICE	4			04		
18	CAS LATENCIES SUPPORTED	2 & 2.5			0C		
19	CS LATENCY	CS latency = 0			01		
20	WE LATENCY	Write latency = 1			02		
21	SDRAM MODULE ATTRIBUTES	Differential CK Input			20		
22	SDRAM DEVICE ATTRIBUTES:GENERAL	NONE			00		
23	SDRAM CYCLE TIME, ^t CK (CAS LATENCY=2)	7.5ns	10 ns 7.5ns	10ns	75	A0 75	A0
24	SDRAM ACCESS FROM CLK, ^t AC (CAS LATENCY=2)	±0.7ns	7.5ns	8ns	70	75	80
25	SDRAM CYCLE TIME, ^t CK (CAS LATENCY=1)	not supported			00		
26	SDRAM ACCESS FROM CLK, ^t AC (CAS LATENCY=1)	not supported			00		
27	MINIMUM ROW PRECHARGE TIME, ^t RP	18ns	20ns	20ns	48	50	50
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, ^t RRD	12ns	15ns	15ns	30	3C	3C
29	MINIMUM RAS# TO CAS# DELAY, ^t RCD	18ns	20ns	20ns	48	50	50
30	MINIMUM RAS# PULSE WIDTH, ^t RAS	42ns	45ns	50ns	2A	2D	32
31	MODULE BANK DENSITY	256MB			40		

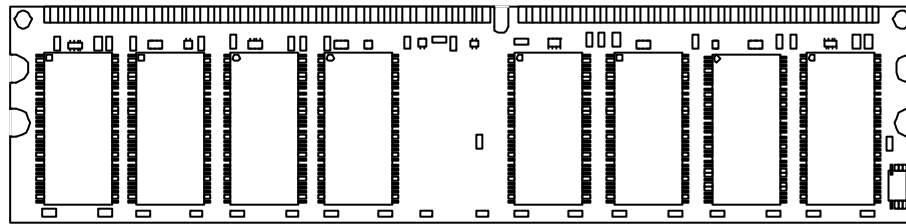
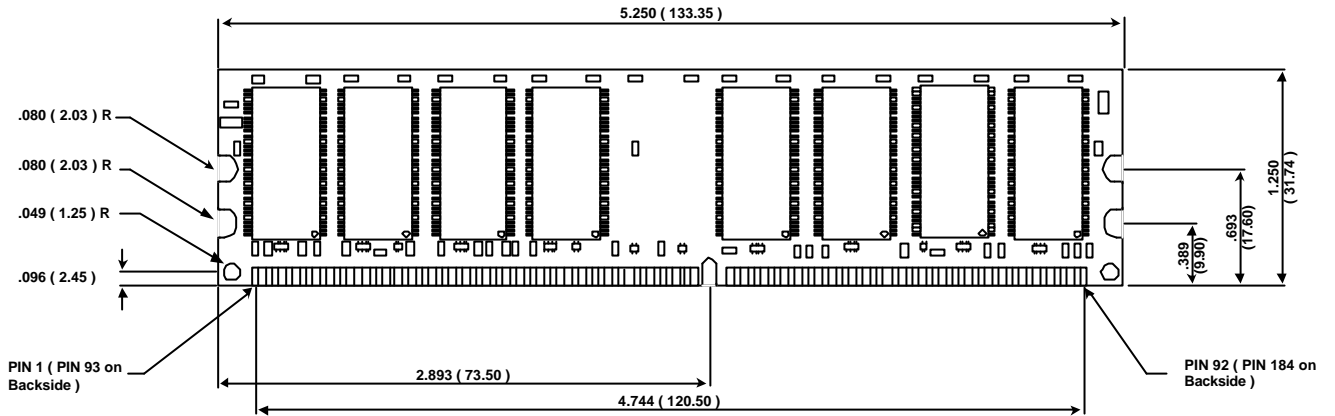
SPD Table / AC Characteristics

SERIAL PRESENCE-DETECT MATRIX

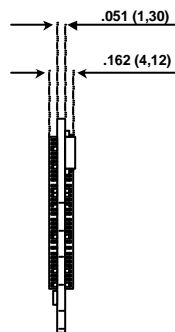
Byte	DESCRIPTION	ENTRY			HEX Code		
		-60	-75 -70	-80	-60	-75 -70	-80
32	COMMAND AND ADDRESS SETUP TIME	0.8 ns	1.0 ns	1.1 ns	80	A0	B0
33	COMMAND AND ADDRESS HOLD TIME	0.8 ns	1.0 ns	1.1 ns	80	A0	B0
34	DATA SIGNAL INPUT SETUP TIME	0.45 ns	0.5 ns	0.6 ns	45	50	60
35	DATA SIGNAL INPUT HOLD TIME	0.45 ns	0.5 ns	0.6 ns	45	50	60
36-40	RESERVED				00		
41	SDRAM DEVICE MIN. ACTIVE/AUTO-REFR. t_{RC}	60 ns	0	0	3C	00	00
42	AUTO REFRESH COMMAND PERIOD t_{RFC}	72 ns	0	0	48	00	00
43	MAX. SDRAM CYCLE TIME t_{CK}	13 ns	0	0	30	00	00
44	DQS-DQ SKEW, DQS TO LAST DQ VALID t_{DQSQ}	0.45	0	0	2D	00	00
45	DATA HOLD SKEW FACTOR t_{QHS}	0.60	0	0	60	00	00
46-61	RESERVED				00		
62	SPD REVISION	0			00		
63	CHECKSUM FOR BYTE 0-62	To be calculated			XX		
64-71	MANUFACTURE'S JEDEC ID CODE	SIEMENS AG			7F 7F 2F 00 00 00 00 00		
72	Manufacturer's Location	Not used			00		
73-90	Manufacturer's Part Number (1 st part)	SDU06464C1B...			XX		
91-92	Manufacturer specific Rev. Code	Not used			00		
93-94	Manufacturing Date	Date			XX		
95-98	Assembly Serial Number	To be calculated			XX		
99-125	Manufacturer specific data	Not used			00		
126	RESERVED				00		
127	RESERVED				00		

Drawings

**184-PIN DDR DIMM
(2 banks, no ECC)
Front View**



Back View



All dimensions in inches (millimeters)

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