

184-pin PC3200 DDR- SDRAM Module

DIMM 256MB DDR-I PC3200 in TSOP Technique

Features:

- 184-pin 64-bit Dual-In-Line Memory Module. Double Date Rate synchronous DRAM Modules for desktop applications.
- DDR- SDRAM component base: 32M8 Infineon or Micron
- $V_{DD} 2,6 \pm 0.2V$, $V_{DDQ} 2,6 \pm 0.2V$
- Programmable CAS Latency, Burst Length and Wrap Sequence
- Auto Refresh (CBR) and Self Refresh
- 8k Refresh every 64ms
- 2.6 I/O (SSTL_2 compatible)
- Serial Presence Detect with EEPROM
- Gold-contact pad
- This module family is fully pin and functional compatible to the JEDEC PC3200 spec. (refer to www.jedec.org)

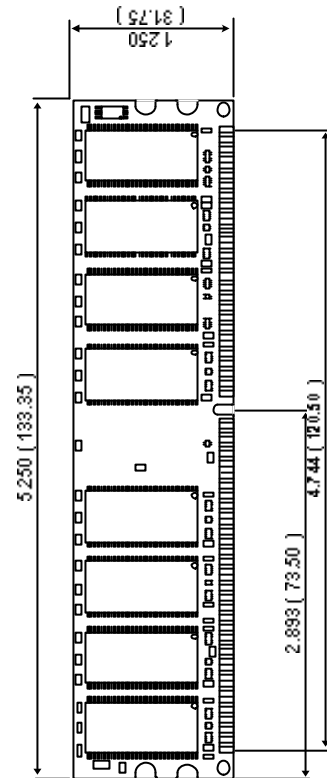


Figure 1: Mechanical Dimensions

Table 1: Order Information / Addressing

Organization	Banks	JEDEC Code	Addressing	Chip code	Swissbit Code
32M x 64 / 8x32x8	1	256MB PC3200S-333	13 / 2 / 10	MT46V32M8TG-5T	SDU03264BxB31MT-50
32M x 64 / 8x32x8	1	256MB PC3200S-333	13 / 2 / 10	HYB25D256800BT-5	SDU03264BxB21IN-50

Table 2: Operating Current ($T_A = 0$ to 70°C ; $V_{DD} = 2.5V \pm 0.2V$, $V_{DDQ} = 2.5V \pm 0.2V$)

Parameter	Symbol	MT-50	IN-50	Unit
Operating Current	max. IDD0	1080	720	mA
Precharge Standby Current (Power Down Mode)	max. IDD2P	32	56	mA

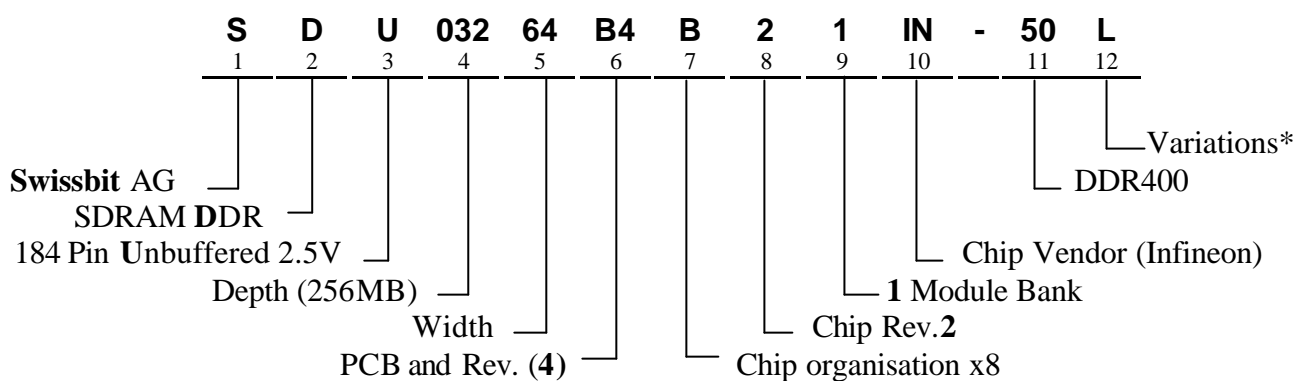
Table 3: AC Characteristics ($T_A = 0$ to 70°C ; $V_{SS} = 0V$; $V_{DD} = 2.5V \pm 0.2V$, $V_{DDQ} = 2.5V \pm 0.2V$)

Parameter	Symbol	MT-50		IN-50		Unit	
		min.	max.	min.	max.		
Clock Cycle Time	t_{CK}	CL = 2.5	6.0	13	6.0	13	ns
		CL = 3.0	5.0	7.5	5.0	7.5	ns
Access Time from Clock	t_{AC}	-0.70	+0.70	-0.70	+0.70	ns	
Row to Column Delay Time	t_{RCD}	15	-	15	-	ns	
Row Precharge Time	t_{RP}	15	-	15	-	ns	

Table 4: Environmental Requirements

Operating Temperature	0°C to + 70°C ambient
Operating Humidity	10% to 90% relative humidity, noncondensing
Operating Pressure	10106 PSI (up to 10000 ft.)
Storage Temperature	-40°C to 70°C
Storage Humidity	5% to 95% without condensing
Storage Pressure	1682 PSI (up to 5000 ft.) at 50°C

Part Number Code



* optional / additional information

SERIAL PRESENCE-DETECT MATRIX

Byte	DESCRIPTION	ENTRY			HEX Code		
		IN-50	MT-50	-	IN-50	MT-50	-
0	NUMBER OF BYTES USED	128			80		
1	TOTAL NUMBER OF SPD MEMORY BYTES	256			08		
2	MEMORY TYPE	DDR-SDRAM			07		
3	NUMBER OF ROW ADDRESSES	13			0D		
4	NUMBER OF COLUMN ADDRESSES	10			0A		
5	NUMBER OF BANKS	1			01		
6	MODULE DATA WIDTH	64			40		
7	MODULE DATA WIDTH (continued)	0			00		
8	MODULE VOLTAGE INTERFACE LEVELS	SSTL_2 2.5V			04		
9	SDRAM CYCLE TIME at CL=3.0	5.0ns			50		
10	SDRAM ACCESS TIME FROM CLOCK (CL=3.0)	0.50ns	0.7ns		50	70	-
11	MODULE CONFIGURATION TYPE	None ECC			00		
12	SELF REFRESH RATE / TYPE	7.8µs			82		
13	SDRAM WIDTH (PRIMARY SDRAM)	x8			08		
14	ERROR-CHECKING SDRAM DATA WIDTH	NONE			00		
15	MINIMUM CLOCK DELAY, t_{CCD}	$t_{CCD} = CKL 1$			01		
16	BURST LENGTH SUPPORTED	2,4,8			0E		
17	NUMBER OF BANKS ON SDDRAM DEVICE	4			04		
18	CAS LATENCIES SUPPORTED	2.0, 2.5, 3.0			1C		
19	CS LATENCY	CS latency = 0			01		
20	WE LATENCY	Write latency = 1			02		
21	SDRAM MODULE ATTRIBUTES	unbuffered			20		
22	SDRAM DEVICE ATTRIBUTES:GENERAL	-			C1		
23	SDRAM CYCLE TIME, t_{CK} (CAS LATENCY=2.5)	6.0 ns	6.0 ns	-	60	60	-
24	SDRAM ACCESS TIME FROM CLOCK (CL=2.5)	0.5 ns	0.7ns	-	50	70	-
25	SDRAM CYCLE TIME, t_{CK} (CAS LATENCY=2.0)	7.5 ns	7.5 ns	-	75	75	-
26	SDRAM ACCESS TIME FROM CLOCK (CL=2.0)	0.5 ns	0.75 ns	-	50	75	-
27	MINIMUM ROW PRECHARGE TIME, t_{RP}	15 ns	15 ns	-	3C	3C	-
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, t_{RRD}	10 ns	10 ns	-	28	28	-
29	MINIMUM RAS# TO CAS# DELAY, t_{RCD}	15 ns	15 ns	-	3C	3C	-
30	MINIMUM RAS# PULSE WIDTH, t_{RAS}	40 ns	40 ns	-	28	28	-
31	MODULE BANK DENSITY	256MB			40		
32	COMMAND AND ADDRESS SETUP TIME t_{IS}	0.6 ns	0.6 ns	-	60	60	-
33	COMMAND AND ADDRESS HOLD TIME	0.6 ns	0.6 ns	-	60	60	-
34	DATA SIGNAL INPUT SETUP TIME	0.4 ns	0.4 ns	-	40	40	-
35	DATA SIGNAL INPUT HOLD TIME	0.4 ns	0.4 ns	-	40	40	-
36-40	RESERVED	-			00		
41	MINIMUM ACTIVE AUTO-REFRESH TIME, t_{RC}	55 ns	55 ns	-	37	37	-
42	AUTO REFRESH COMMAND PERIOD t_{RFC}	65 ns	70 ns	-	41	46	-
43	MAX. SDRAM CYCLE TIME t_{CKmax}	10 ns	12 ns	-	28	30	-
44	DQS-DQ SKEW, DQS TO LAST DQ VALID t_{DQSQ}	0.4 ns	0.4 ns	-	28	28	-
45	DATA HOLD SKEW FACTOR t_{OHS}	0.5 ns	0.5 ns	-	50	50	-
46-61	RESERVED, not used	-			00		
62	SPD REVISION	Release 1.1			11		
63	CHECKSUM FOR BYTE 0-62	-	-	-	BF	80	-
64-71	MANUFACTURE'S JEDEC ID CODE	Swissbit AG / SIEMENS AG			7F 7F 2F ..		
72	Manufacturer's Location	Not used			00		
73-90	Manufacturer's Part Number (1 st part)	SDU03264B...			xx		
91-127	Manufacturer specific data	-			xx		

Swissbit Group Adresses:

Swissbit AG

Industriestrasse 4 – 8
CH – 9552 Bronschhofen
Switzerland

Phone: +41 (0)71 913 72 66
Fax: +41 (0)71 913 74 50

Swissbit Germany GmbH

Wolfener Strasse 36
D – 12681 Berlin
Germany

Phone: +49 (0)30 93 69 54 – 0
Fax: +49 (0)30 93 69 54 – 55

Swissbit NA, Inc.

18 Willett Avenue, Suite 203
Port Chester, NY 10573
USA

Phone: +1 914 935 1400
Fax: +1 914 935 9865

Swissbit NA, Inc.

7801 North Lamar Boulevard, Suite E – 186
Austin, TX 78752
USA

Phone: +1 512 302 9001
Fax: +1 512 302 4808