

184-pin PC2700 DDR- SDRAM Module
DIMM 256MB DDR-I PC2700 in TSOP Technique

- Features:**
- 184-pin 64-bit Dual-In-Line Memory Module. Double Date Rate synchronous DRAM Modules for desktop applications.
 - DDR- SDRAM component base: 32M8 Infineon or Micron
 - $V_{DD} 2.5 \pm 0.2V$, $V_{DDQ} 2.5 \pm 0.2V$
 - Programmable CAS Latency, Burst Length and Wrap Sequence
 - Auto Refresh (CBR) and Self Refresh
 - 8k Refresh every 64ms
 - 2.6 I/O (SSTL_2 compatible)
 - Serial Presence Detect with EEPROM
 - Gold-contact pad
 - This module family is fully pin and functional compatible to the JEDEC PC2700 spec. (refer to www.jedec.org)

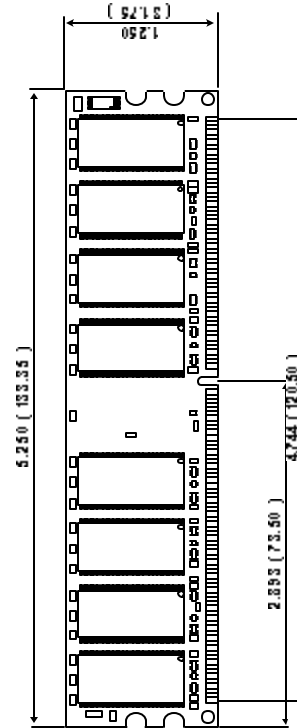


Figure 1: Mechanical Dimensions

Table 1: Order Information / Addressing

Organization	Banks	JEDEC Code	Addressing	Chip code	Swissbit Code
32M x 64 / 8x32x8	1	256MB PC2700-2,533	13 / 2 / 10	MT46V32M8TG -6	SDU03264BxB31MT-60
32M x 64 / 8x32x8	1	256MB PC2700-2,533	13 / 2 / 10	HYB25D256800BT -6	SDU03264BxB21IN-60

Table 2: Operating Current ($T_A = 0$ to 70°C ; $V_{DD} = 2.5V \pm 0.2V$, $V_{DDQ} = 2.5V \pm 0.2V$)

Parameter	Symbol	MT-60	IN-60	Unit
Operating Current	max. IDD0	1080	720	mA
Precharge Standby Current (Power Down Mode)	max. IDD2P	32	56	mA

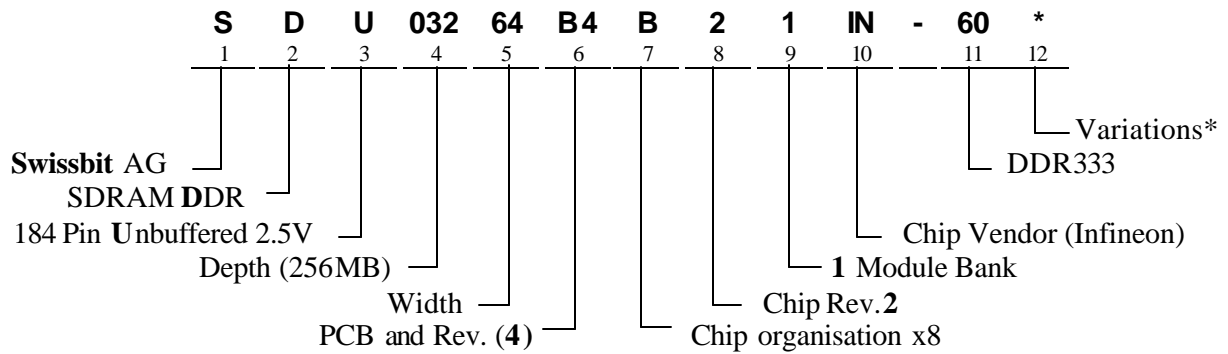
Table 3: AC Characteristics ($T_A = 0$ to 70°C ; $V_{SS} = 0V$; $V_{DD} = 2.5V \pm 0.2V$, $V_{DDQ} = 2.5V \pm 0.2V$)

Parameter	Symbol	MT-60		IN-60		Unit
		min.	max.	min.	max.	
Clock Cycle Time	t_{CK}	6.0	12	6.0	12	ns
		7.5	12	7.5	12	ns
Access Time from Clock	t_{AC}	-0.70	+0.70	-0.70	+0.70	ns
Row to Column Delay Time	t_{RCD}	18	-	18	-	ns
Row Precharge Time	t_{RP}	18	-	18	-	ns

Table 4: Environmental Requirements

Operating Temperature	0°C to + 70°C ambient
Operating Humidity	10% to 90% relative humidity, noncondensing
Operating Pressure	10106 PSI (up to 10000 ft.)
Storage Temperature	-40°C to 70°C
Storage Humidity	5% to 95% without condensing
Storage Pressure	1682 PSI (up to 5000 ft.) at 50°C

Part Number Code



* optional / additional information

SERIAL PRESENCE-DETECT MATRIX

Byte	DESCRIPTION	ENTRY			HEX Code		
		IN-60	MT-60	-	IN-60	MT-60	-
0	NUMBER OF BYTES USED	128			80		
1	TOTAL NUMBER OF SPD MEMORY BYTES	256			08		
2	MEMORY TYPE	DDR-SDRAM			07		
3	NUMBER OF ROW ADDRESSES	13			0D		
4	NUMBER OF COLUMN ADDRESSES	10			0A		
5	NUMBER OF BANKS	1			01		
6	MODULE DATA WIDTH	64			40		
7	MODULE DATA WIDTH (continued)	0			00		
8	MODULE VOLTAGE INTERFACE LEVELS	SSTL_2 2.5V			04		
9	SDRAM CYCLE TIME at CL=3.0	6.0ns			60		
10	SDRAM ACCESS TIME FROM CLOCK (CL=3.0)	0.7ns	0.7ns		70	70	-
11	MODULE CONFIGURATION TYPE	None ECC			00		
12	SELF REFRESH RATE / TYPE	7.8µs			82		
13	SDRAM WIDTH (PRIMARY SDRAM)	x8			08		
14	ERROR-CHECKING SDRAM DATA WIDTH	NONE			00		
15	MINIMUM CLOCK DELAY, ' CCD	t _{ccd} = CKL 1			01		
16	BURST LENGTH SUPPORTED	2,4,8			0E		
17	NUMBER OF BANKS ON SDDRAM DEVICE	4			04		
18	CAS LATENCIES SUPPORTED	2.0, 2.5			0C		
19	CS LATENCY	CS latency = 0			01		
20	WE LATENCY	Write latency = 1			02		
21	SDRAM MODULE ATTRIBUTES	unbuffered			20		
22	SDRAM DEVICE ATTRIBUTES:GENERAL	-			C0	C0	-
23	SDRAM CYCLE TIME, t _{CK} (CAS LATENCY=2.5)	7.5 ns	7.5 ns	-	75	75	-
24	SDRAM ACCESS TIME FROM CLOCK (CL=2.5)	0.7 ns	0.7ns	-	70	70	-
25	SDRAM CYCLE TIME, t _{CK} (CAS LATENCY=2.0)	-	-	-	00	00	-
26	SDRAM ACCESS TIME FROM CLOCK (CL=2.0)	-	-	-	00	00	-
27	MINIMUM ROW PRECHARGE TIME, t _{RP}	18 ns	18 ns	-	48	48	-
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, t _{RRD}	12 ns	12 ns	-	30	30	-
29	MINIMUM RAS# TO CAS# DELAY, t _{RCD}	18 ns	18 ns	-	48	48	-
30	MINIMUM RAS# PULSE WIDTH, t _{RAS}	42 ns	42 ns	-	2A	2A	-
31	MODULE BANK DENSITY	256MB			40		
32	COMMAND AND ADDRESS SETUP TIME t _{IS}	0.75 ns	0.8 ns	-	75	80	-
33	COMMAND AND ADDRESS HOLD TIME	0.75 ns	0.8 ns	-	75	80	-
34	DATA SIGNAL INPUT SETUP TIME	0.45 ns	0.45 ns	-	45	45	-
35	DATA SIGNAL INPUT HOLD TIME	0.45 ns	0.45 ns	-	45	45	-
36-40	RESERVED	-			00		
41	MINIMUM ACTIVE AUTO-REFRESH TIME, t _{RC}	60 ns	60 ns	-	3C	3C	-
42	AUTO REFRESH COMMAND PERIOD t _{RFC}	72 ns	72ns	-	48	48	-
43	MAX. SDRAM CYCLE TIME t _{CKmax}	12 ns	12 ns	-	30	30	-
44	DQS-DQ SKEW, DQS TO LAST DQ VALID t _{DQSQ}	0.45 ns	0.45 ns	-	2D	2D	-
45	DATA HOLD SKEW FACTOR t _{QHS}	0.55 ns	0.55 ns	-	55	55	-
46-61	RESERVED, not used	-			00		
62	SPD REVISION	-			00	10	
63	CHECKSUM FOR BYTE 0-62	-	-	-	00	27	-
64-71	MANUFACTURE'S JEDEC ID CODE	Swissbit AG			7F 7F 7F DA		
72	Manufacturer's Location	Not used			00		
73-90	Manufacturer's Part Number (1 st part)	SDU03264B...			xx		
91-127	Manufacturer specific data	-			xx		

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